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1 [Instruction path coprocessors](#)

Yuan Chou, John Paul Shen

May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

Full text available: pdf(134.64 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper presents the concept of an Instruction Path Coprocessor (I-COP), which is a programmable on-chip coprocessor, with its own mini-instruction set, that operates on the core processor's instructions to transform them into an internal format that can be more efficiently executed. It is located off the critical path of the core processor to ensure that it does not negatively impact the core processor's cycle time or pipeline depth. An I-COP is highly versatile and can be used ...

2 [High performance messaging on workstations: Illinois fast messages \(FM\) for Myrinet](#)

Scott Pakin, Mario Lauria, Andrew Chien

December 1995 **Proceedings of the 1995 ACM/IEEE conference on Supercomputing (CDROM)**

Full text available: pdf(250.56 KB)
 html(3.37 KB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

3 [Issues in partitioning & design space exploration for codesign: Dynamic hardware/software partitioning: a first approach](#)

Greg Stitt, Roman Lysecky, Frank Vahid

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(215.05 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Partitioning an application among software running on a microprocessor and hardware co-processors in on-chip configurable logic has been shown to improve performance and energy consumption in embedded systems. Meanwhile, dynamic software optimization methods have shown the usefulness and feasibility of runtime program optimization, but those optimizations do not achieve as much as partitioning. We introduce a first approach to dynamic hardware/software partitioning. We describe our system archit ...

Keywords: FPGA, codesign, dynamic optimization, embedded systems, hardware/software partitioning, platforms, self-improving chips, synthesis, system-on-a-chip

4 Simulation and architecture evaluation: Vector vs. superscalar and VLIW architectures for embedded multimedia benchmarks

Christoforos Kozyrakis, David Patterson

November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Full text available:  pdf(1.34 MB) 

[Publisher Site](#)


Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Multimedia processing on embedded devices requires an architecture that leads to high performance, low power consumption, reduced design complexity, and small code size. In this paper, we use EEMBC, an industrial benchmark suite, to compare the VIRAM vector architecture to superscalar and VLIW processors for embedded multimedia applications. The comparison covers the VIRAM instruction set, vectorizing compiler, and the prototype chip that integrates a vector processor with DRAM main memory. We de ...

5 Towards nanocomputer architecture

Paul Beckett, Andrew Jennings

January 2002 **Australian Computer Science Communications , Proceedings of the seventh Asia-Pacific conference on Computer systems architecture - Volume 6**, Volume 24 Issue 3

Full text available:  pdf(1.24 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

At the nanometer scale, the focus of micro-architecture will move from processing to communication. Most general computer architectures to date have been based on a "stored program" paradigm that differentiates between memory and processing and relies on communication over busses and other (relatively) long distance mechanisms. Nanometer-scale electronics --- nanoelectronics - promises to fundamentally change the ground-rules. Processing will be cheap and plentiful, interconnection expensive but ...

Keywords: MIMD, QCA, SIMD, array architecture, computer architecture, device scaling, future trends, micro-architecture, nanocomputer architecture, nanoelectronic technology

6 Virtual machine monitors: Terra: a virtual machine-based platform for trusted computing

Tal Garfinkel, Ben Pfaff, Jim Chow, Mendel Rosenblum, Dan Boneh

October 2003 **Proceedings of the nineteenth ACM symposium on Operating systems principles**

Full text available:  pdf(140.31 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)


We present a flexible architecture for trusted computing, called Terra, that allows applications with a wide range of security requirements to run simultaneously on commodity hardware. Applications on Terra enjoy the semantics of running on a separate, dedicated, tamper-resistant hardware platform, while retaining the ability to run side-by-side with normal applications on a general-purpose computing platform. Terra achieves this synthesis by use of a *trusted virtual machine monitor* (TVMM) ...

Keywords: VMM, attestation, authentication, trusted computing, virtual machine, virtual machine monitor

7 Attacking the semantic gap between application programming languages and configurable hardware

Greg Snider, Barry Shackleford, Richard J. Carter

February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**


Full text available:  pdf(258.65 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

It is difficult to exploit the massive, fine-grained parallelism of configurable hardware with a conventional application programming language such as C, Pascal or Java. The difficulty arises from the mismatch between the synchronous, concurrent processing capability of the hardware and the expressiveness of the language—the so-called "semantic gap." We attack this problem by using a programming model matched to the hardware's capabilities that can be implemented in any (unmodified) object ...

8 **FunState—an internal design representation for codesign**

L. Thiele, K. Strehl, D. Ziegenbein, R. Ernst, J. Teich

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**


Full text available:  pdf(253.83 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper, an internal design model called FunState (functions driven by state machines) is presented that enables the representation of different types of system components and scheduling mechanisms using a mixture of functional programming and state machines. It is shown here how properties relevant for scheduling and verification of specification models like boolean dataflow, cyclostatic dataflow, synchronous dataflow, marked graphs, and communicating state ...

9 **VISA: Netstation's virtual Internet SCSI adapter**

Rodney Van Meter, Gregory G. Finn, Steve Hotz

October 1998 **Proceedings of the eighth international conference on Architectural support for programming languages and operating systems**, Volume 32, 33
Issue 5, 11

Full text available:  pdf(1.23 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper we describe the implementation of VISA, our Virtual Internet SCSI Adapter. VISA was built to evaluate the performance impact on the host operating system of using IP to communicate with peripherals, especially storage devices. We have built and benchmarked file systems on VISA-attached emulated disk drives using UDP/IP. By using IP, we expect to take advantage of its scaling characteristics and support for heterogeneous media to build large, long-lived systems. Detailed file system ...

10 **Software engineering for security: a roadmap**

Premkumar T. Devanbu, Stuart Stubblebine

May 2000 **Proceedings of the conference on The future of Software engineering**

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Keywords: copy protection, security, software engineering, water-marking

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1 Store-and-forward message switching using polar-orbiting microsatellites

Ward, J.W.;

Message Handling - Past, Present and Future, IEE Colloquium on , 11 Nov 1991
 Pages:9/1 - 9/4

[\[Abstract\]](#) [\[PDF Full-Text \(224 KB\)\]](#) **IEE CNF**

2 ClassiPI: an architecture for fast and flexible packet classification

Iyer, S.; Rao Kompella, R.; Shelat, A.;

Network, IEEE , Volume: 15 , Issue: 2 , March-April 2001
 Pages:33 - 41

[\[Abstract\]](#) [\[PDF Full-Text \(136 KB\)\]](#) **IEEE JNL**

3 A video display processing platform for future TV concepts

de With, P.H.N.; Jaspers, E.G.T.; van Meerbergen, J.L.; Timmer, A.H.; Strik, T.J.;

Consumer Electronics, IEEE Transactions on , Volume: 45 , Issue: 4 , Nov 1999
 Pages:1230 - 1240

[\[Abstract\]](#) [\[PDF Full-Text \(836 KB\)\]](#) **IEEE JNL**

4 Hardware and software implications of representing scenes as data

Bove, V.M., Jr.;

Acoustics, Speech, and Signal Processing, 1993. ICASSP-93., 1993 IEEE International Conference on , Volume: 1 , 27-30 April 1993
 Pages:121 - 124 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(316 KB\)\]](#) **IEEE CNF**

5 Comparison of spectral index, semi-vectorial finite difference and vector finite element methods for the modal analysis of semiconductor optical rib waveguides

Stern, M.S.;

Computation in Electromagnetics, 1991., International Conference on , 25-27 Nov 1991

Pages:18 - 21

[\[Abstract\]](#) [\[PDF Full-Text \(252 KB\)\]](#) IEEE CNF

6 DiffServ edge routers over network processors: implementation and evaluation

Ying-Dar Lin; Yi-Neng Lin; Shun-Chin Yang; Yu-Sheng Lin;

Network, IEEE , Volume: 17 , Issue: 4 , July-Aug. 2003

Pages:28 - 34

[\[Abstract\]](#) [\[PDF Full-Text \(592 KB\)\]](#) IEEE JNL

7 High-speed data paths in host-based routers

Walton, S.; Hutton, A.; Touch, J.;

Computer , Volume: 31 , Issue: 11 , Nov. 1998

Pages:46 - 52

[\[Abstract\]](#) [\[PDF Full-Text \(216 KB\)\]](#) IEEE JNL

8 An adaptive current control scheme for PWM synchronous motor drives: analysis and simulation

Le-Huy, H.; Dessaint, L.A.;

Power Electronics, IEEE Transactions on , Volume: 4 , Issue: 4 , Oct. 1989

Pages:486 - 495

[\[Abstract\]](#) [\[PDF Full-Text \(728 KB\)\]](#) IEEE JNL

9 The Aleph event builder: a multi-user FASTBUS master

Einsweiler, K.; Marchioro, A.; von Ruden, W.; Battaiotto, P.;

Nuclear Science, IEEE Transactions on , Volume: 35 , Issue: 1 , Feb 1988

Pages:316 - 320

[\[Abstract\]](#) [\[PDF Full-Text \(288 KB\)\]](#) IEEE JNL

10 A real-world approach to benchmarking DSP real-time operating systems

Keate, L.;

WESCON/97. Conference Proceedings , 4-6 Nov. 1997

Pages:418 - 424

[\[Abstract\]](#) [\[PDF Full-Text \(496 KB\)\]](#) IEEE CNF

11 High speed video board as a case study for hardware-software co-design

Herrmann, D.; Maas, E.; Trawny, M.; Ernst, R.; Ruffer, P.; Seitz, M.; Hasenzahl, S.;

Computer Design: VLSI in Computers and Processors, 1996. ICCD '96.

Proceedings., 1996 IEEE International Conference on , 7-9 Oct. 1996
Pages:185 - 190

[\[Abstract\]](#) [\[PDF Full-Text \(712 KB\)\]](#) IEEE CNF

12 Information assurance for enterprise fiber optic networks

DeCusatis, C.;

Information Assurance Workshop, 2003. IEEE Systems, Man and Cybernetics Society , 18-20 June 2003

Pages:282 - 287

[\[Abstract\]](#) [\[PDF Full-Text \(705 KB\)\]](#) IEEE CNF

13 Kernel formation in Garpcc

Callahan, T.;

Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on , 9-11 April 2003

Pages:308 - 309

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14 A rule grouping technique for weight-based TCAM coprocessors [packet classification application]

Che, H.; *Wang, Y.;* *Wang, Z.;*

High Performance Interconnects, 2003. Proceedings. 11th Symposium on , 20-22 Aug. 2003

Pages:32 - 37

[\[Abstract\]](#) [\[PDF Full-Text \(471 KB\)\]](#) IEEE CNF

15 Robust media processing in a flexible and cost-effective network of multi-tasking coprocessors

Rutten, M.J.; *van Eijndhoven, J.T.J.;* *Pol, E.-J.D.;*

Real-Time Systems, 2002. Proceedings. 14th Euromicro Conference on , 19-21 June 2002

Pages:223 - 230

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A Quantitative Analysis of Reconfigurable **Coprocessors** for Multimedia Applications Takashi Miyamori
ogun.stanford.edu/publications/FCCM.ps.gz

[Coproprocessor Codesign for Programmable Architectures - Mishra, Rousseau, Dutt..](#) (Correct)

Dep. Inf. Comp. Sc. Univ. California, Irvine **Coprocessor** Codesign for Programmable Architectures
tima.imag.fr/publications/files/rr/ccp_160.pdf

[Exploiting Reconfigurable FPGA for Parallel Query.. - Leung, Ercegovic, Muntz](#) (Correct)

Gate Arrays (FPGAs)an SRAM-based FPGA **coprocessor**, for query processing in computation-intensive
www.ucop.edu/research/micro/97_98/97_126.pdf

[National Science Foundation Phase I Final Report - Program Official](#) (Correct)

Number: DMI-9461912 Agent-Based Integration of **Legacy** and Reusable Software Systems Phase II
ftp.bbtech.com/pub/gbb/papers/nsf-sbir-94-final.ps

[Performance Comparison Of Video Transport Over ATM.. - Hossain, Kang, Horst](#) (Correct)

group has developed fully functional 800Mbps ATM **switch** [2] along with software video applications (such as this VS) which generate traffic through the **switch**. Our Video Server (VS) is a multimedia storage Send END Signal to Client Receive Thread iPOINT **Switch** Video Server No Client request Send compressed berserk.vlsi.uiuc.edu/people/ashfaq/ieee.mm97.ps

[A hardware supported system for Kohonen's Selforganizing Map - Thole, Speckmann.. \(1993\)](#) (Correct)

system consisting of different parts. A neural **coprocessor** (COKOS) is connected to a personal computer
www-ti.informatik.uni-tuebingen.de/~speckman/.papers/edinburgh93.ps

[Making the future safe for the past: Adding.. - Bracha, Odersky.. \(1998\)](#) (Correct) (78 citations)

generic types on top of Smalltalk. The generic **legacy** problem However, few proposals tackle the generic
www.cs.bell-labs.com/who/wadler/topics/..papers/gj-oopsla/gj-oopsla-letter.ps.gz

[Architecture Description Language Driven Design Space .. - Mishra, Rousseau.. \(2001\)](#) (Correct)

Design Space Exploration in the Presence of **Coprocessors** Prabhat Mishra y Frederic Rousseau z Nikil
www.cecs.uci.edu/~copper/publications/sasimi2001.pdf

[High Performance Messaging on Workstations: Illinois Fast.. - Pakin, Lauria, Chien \(1995\)](#) (Correct) (223 citations)

the division of labor between host and network **coprocessor**, management of the input/output (I/O) bus, to compare against [15]TCP/IP is a **legacy** protocol in widespread use. And the Illinois All measurements were taken on an 8-port Myrinet **switch** and a pair of workstations (see Section 2)In
www-csag.ucsd.edu/papers/csag/external/myrinet-fm-sc95.ps

[High Performance Messaging on Workstations: - Illinois Fast Messages](#) (Correct)

the division of labor between host and network **coprocessor**, management of the input/output (I/O) bus, and to compare against [15]TCP/IP is a **legacy** protocol in widespread use. And the Illinois All measurements were taken on an 8-port Myrinet **switch** and a pair of workstations (see Section 2)In
www.supercomp.org/sc95/proceedings/567_SPAK/SC95.PS

[Coprocessors for special neural networks KOKOS and KOBOLD - Speckmann, Thole..](#) (Correct)

Coprocessors for special neural networks KOKOS and KOBOLD
www-ti.informatik.uni-tuebingen.de/~speckman/.papers/icnn94.ps

[Rapid Prototyping with Reconfigurable Hardware for.. - Golatowski..](#) (Correct)

2. Description of a reconfigurable scheduling **coprocessor** 3. First performance evaluation and comparison other functionality of the scheduler like context **switch**, event registration or handling of resource the minimum time interval between two task **switches**. The C-andD- parameters are measured in www.cse.unl.edu/rtss98wip/proceedings/Golatowski.ps

Hardware-Software Codesign for Dynamically Reconfigurable.. - Chatha, Vemuri (1999) (Correct) (1 citation)
processor, a dynamically reconfigurable hardware **coprocessor** and memory elements. The problem comprises of www.ece.uc.edu/~ddel/publications/chatha-fpl-99.ps

Design of Multi-Tasking Coprocessor Control for Eclipse - Rutten, van Eindhoven, Pol (2002) (Correct)
Design of Multi-Tasking **Coprocessor** Control for Eclipse Martijn J. Rutten Jos T.J.
www.sigda.org/Archives/ProceedingArchives/Codes/Codes2002/papers/2002/codes02/htmlfiles/sun_sgi/.../pdffiles/5_4.p

Performance Evaluation and Modeling of MPI Communications .. - Folino, Spezzano, Talia (Correct)
of one or more Sparc processors, a communication **coprocessor**, the Elan processor, that connects each node a fat tree network built from Meiko 8x8 crosspoint **switches** [4]The CS-2 network provides a bi-sectional
isi-cnr.deis.unical.it:1080/~talia/hpcn98.ps

Optimal Multicast with Packetization and Network Interface.. - Kesavan, Panda (1997) (Correct) (5 citations)
support for nodes, which typically includes a **coprocessor** and memory, to implement the lower layers of conventional binomial tree on a 64-node irregular **switch**-based network using simulation experiments. trees with minimal contention on irregular **switch**-based networks. 5 Performance Analysis In this
ftp.cis.ohio-state.edu/pub/communication/papers/icpp97-packet_mcast.ps.Z

Mechanisms and Interfaces for Software-Extended Coherent Shared.. - Chaiken (1994) (Correct) (3 citations)
SPARC architecture [72]and a floating-point **coprocessor**. The nodes communicate via messages through a This implementation allows the processor to **switch** quickly between the different threads of upon a remote memory access. While the context-**switching** mechanism is intended to help the system
ftp.cag.lcs.mit.edu/pub/papers/chaiken-dissert-1-10.ps.Z

Secure Coprocessors in Electronic Commerce Applications - Yee, Tygar (1995) (Correct) (25 citations)
Secure **Coprocessors** in Electronic Commerce Applications Bennet
www.cs.ucsd.edu/users/bsy/pub/ecommerce.ps.gz

Intelligent Computing About Complex Dynamical Systems - Zhao (1994) (Correct)
the controllable region of the system and the **switching** surfaces where control parameters should of four segments, each of which starts at a **switching** state marked as a small circle the reference Control Law specifying the time instance, **switching** state, and corresponding control value for
www.cis.ohio-state.edu/insight/papers/mcs.ps

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[Towards a Crystal Ball for Data Retrieval - Hellerstein \(Correct\)](#)

that the response fit the query. This is the **legacy** of years of research into supporting
s2k-ftp.cs.berkeley.edu/postgres/papers/ngits97-control.ps.Z

[Learning Planning Operators by Observation and Practice - Wang \(1994\) \(Correct\) \(12 citations\)](#)

www.rpal.rockwell.com/~mei/aips94.ps

[FPGA Based Prototyping for Verification and.. - Benner, Ernst.. \(Correct\)](#)

www.ida.ing.tu-bs.de/research/publications/ps/BEK+94:FPGA_BasedProtoVerif.ps.gz

[Formalising Abilities and Opportunities of Agents - van Linder, van der Hoek, Meyer \(1998\) \(Correct\) \(2 citations\)](#)

ftp.cs.uu.nl/pub/RUU/CS/techreps/CS-1998/1998-08.ps.gz

[Beyond Digital Naturalism - Fontana, Wagner, Buss \(1994\) \(Correct\) \(9 citations\)](#)

growth of object species i. It is convenient to **switch** to internal coordinates or relative frequencies,
www.santafe.edu/~walter/Papers/digitalnat.US.ps.gz

[Development, Learning and Evolution in Animats - Kodjabachian, Meyer \(1994\) \(Correct\) \(2 citations\)](#)

occurs at the time of first cleavage, which **switches** a bit of the Boolean network state vector into
www.biologie.ens.fr/fr/animatlab/perso/kodjaba/jkjamperac.ps.gz

[An Object Calculus with Algebraic Rewriting - Compagnoni, Fernández \(Correct\)](#)

www.ens.fr/~maribel/papers/PLILP97.ps.gz

[Statistical Learning, Localization, and Identification of.. - Hornegger, Niemann \(1995\) \(Correct\) \(1 citation\)](#)

www5.informatik.uni-erlangen.de/TeX/Literatur/ps-dir/1995/Hornegger95:SLL.ps.gz

[Fourth And Fifth Order Efficiency: Fisher Information - Kano \(Correct\)](#)

koko15.hus.osaka-u.ac.jp/members/kano/research/.dvi/fisher.ps

[Frames, Objects and Relations: Three Semantic.. - Norrie, Reimer.. \(1994\) \(Correct\)](#)

www.globis.ethz.ch/publications/docs/1994d-nrlrs-krdb.ps.gz

[Towards 3-D model-based tracking and recognition of human.. - Gavrilă, Davis \(1995\) \(Correct\)](#)

www.umiacs.umd.edu/users/gavrilă/iwafgr.ps.Z

[Uniform Reconstruction of Gaussian Processes - Müller-Gronbach, Ritter \(1995\) \(Correct\) \(1 citation\)](#)

ftp.math.fu-berlin.de/pub/math/publ/pre/1995/pr-a-95-26.ps.Z

[Topic Detection and Tracking Pilot Study - Allan, Carbonell, Doddington.. \(1998\) \(Correct\)](#)

Loop through the stories again, but now consider **switching** each story from its present topic to the
were folded into a single number, the topic-**switch** penalty, which was imposed whenever the topic
topic changed between frames/sentences. The topic-**switch** penalty was tuned to produce the correct average
www.cs.cmu.edu/~yiming/papers.yy/tdt1-final-report.ps

[The Alloc Stream Facility: A Redesign of Application-Level .. - Krieger, Stumm, Unrau \(1994\) \(Correct\) \(9 citations\)](#)

processors need to save and restore on context **switches**. But it can also be due to new operating system
mode is specified on each call, instead of **switching** between stream modes with set alloc mode.
must execute special code whenever the application **switches** between reading from and writing to a stream.
ftp.cs.toronto.edu/pub/parallel/Krieger_etal_IEEEComp94.ps.Z

Working Memory and Dyslexia - Fawcett, Baddeley (1992) (Correct)
<ftp://shef.ac.uk/pub/uni/projects/scp/lrgdocs/lrg913.ps>

Segregatory Coordination and Ellipsis in Text Generation - Shaw (1998) (Correct) (6 citations)
www.cs.columbia.edu/~shaw/papers/colingac198.ps.gz

Integrating Temporal, Real-Time, and Active Databases - Ramamritham.. (1996) (Correct) (3 citations)
www-ccs.cs.umass.edu/~sim/sigrec96.ps

Correction of a Memory Management Method for Lock-Free Data.. - Michael, Scott (1995) (Correct) (5 citations)
hypatia.dcs.qmw.ac.uk/data/edu/cs.rochester.edu/systems/95.tr599.Memory_management_for_lock-free_data_structures.ps.gz

Optimizing ML with Run-Time Code Generation - Leone, Lee (1995) (Correct) (91 citations)
process. To avoid the overhead of context **switching** on every packet, a packet filter must be by user-level processes while avoiding context **switches**. Such an approach has also been investigated by
foxnet.cs.cmu.edu/~petel/papers/staged/mleone-pldi96.ps

Approximate Kinodynamic Planning Using L 2 -norm Dynamic Bounds - Reif, Tate (1990) (Correct) (4 citations)
www.cs.unt.edu/~srt/papers/l2motion.ps

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





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